Copyright © 2001, GaAs MANTECH, Inc.

High Density Plasma Etch Processes for the Manufacture of Optoelectronic Devices based on InP

D J Thomas, K Powell, M M Bourke, Y P Song & C Fragos
Trikon Technologies Ltd
Ringland Way, Newport, NP18 2TA, UK
Phone: +44 (0)1633 414000, email: *firstname.lastname*@trikon.com

F R Shepherd & D Ducharme
Nortel Networks, 3500 Carling Ave, MS 043/12/P16, Nepean, ON K2H 8E9, Canada
© 2001 GaAs Mantech

ABSTRACT

This paper describes the use of high density plasma etch systems for the fabrication of long wavelength optoelectronic devices based on InP. In particular it is shown that the combination of a high density inductively coupled plasma (ICP) and a high temperature electro-static chuck (ESC) may be used for both shallow optical waveguides and for deep optical mirrors in InP-based epitaxial layers. It is also shown that a very high density magnetic zero resonant induction (M0RI™) plasma at lower temperatures offers the flexibility and control required for hard-mask open and sidewall 'spacer' etch processes involving dielectric materials.

INTRODUCTION

The optical telecommunications industry is rapidly expanding its network capacity in order to cope with the existing and projected demands for data transmission. The current trend is towards increasing the effective bandwidth by working with multiple wavelengths. 'Dense wavelength division multiplexing' (DWDM) involves moving away from discrete optical components to wafer-scale integrated optical sub-systems such as laser diode arrays incorporating multiplexing waveguide functions, waveguide detectors and high speed modulators. The need for integration, together with increases in the number of discrete devices required on a single wafer, means that there is a move away from R&D systems towards production worthy processes and tooling which can cope with the expected capacity. Such tooling can also offer significant process benefits such as higher and more consistent etch rates, variable profiles and better control over critical dimension and uniformity.

During the manufacture of the majority of InP-based optoelectronic devices there is a need to etch the following :

- Semiconductor layers (normally including InGaAs, InP and InGaAsP, sometimes in the form of multi-quantum wells).
- Dielectrics (for subsequent use as hard-masks or for subsequent contacting with metals).

Here we focus specifically on these application areas.

EXPERIMENTAL

All of the etch experiments were carried out on 3" diameter InP wafers provided by Nortel Networks. The layer structure for each process type is described alongside the results in the next section. In all cases etching was carried out using an Omega® 201 system from Trikon Technologies fitted either with an ICP or a M0RI plasma source. Figure 1 shows a schematic of the ICP tool.

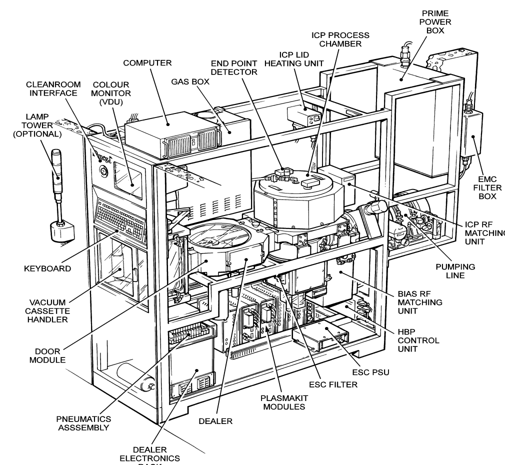

Figure 1 Omega 201 ICP etch system.

The ICP source produces a plasma with a charge density typically in the range 10^{11}-10^{12} cm^{-3} and for these experiments was operated at a pressure of ~5 mtorr. All of the ICP etches involved the use of a high temperature ESC set in the range 150-180 ^{o}C. In contrast the M0RI™ source produces a plasma with a charge density typically 10 times higher than the ICP through the formation of a helicon plasma wave [1]. The helicon wave results from the emersion of the plasma in an electromagnetic field of around 200 G. The M0RI processes were operated at 2.5 mtorr and a conventional (low temperature) ESC was used set to -15 ^{o}C. The ESC designs have been described in detail elsewhere [2].

RESULTS

Waveguide and Mirror Etching

Ridge waveguides are used to confine optical modes as part of larger optical devices. In an active optoelectronic device the simplest way to form an optical waveguide is by etching a shallow feature into the epitaxial layers (typically InGaAs and InP) above the light carrying (or 'active') region that is typically a single layer of InGaAsP or multi-quantum wells comprising InGaAsP. The depth and lateral dimensions of the ridge are typically 1-4 µm. The desired profile will vary depending upon the subsequent processing steps but is typically ~80-85°.

Optical mirrors are created when the etching is continued through the active layer and into the underlying material (usually InP). Here the etch depth is typically 8-10 µm and the profile is required to be as vertical as possible. It is also a general requirement for both the waveguide and mirror etches that the sidewall and 'floor' are as smooth as possible as roughness can lead to inefficient optical propagation.

In order to avoid roughness it is necessary to remove the constituents of an alloy at equal rates. A simple sputtering process would lead to preferential loss of the lightest element (P in the case of InP) and In globules would be left on the wafer. A solution to this by other workers has been to use CH_4/H_2 plasmas where the P is liberated as PH_3 and the In as $In(CH_3)_3$. However the method is subject to significant limitations as follows :

- Etch rates are very low (typically 0.02-0.1 µm/min for InP) making high volume production processes impractical.
- The etch chamber and wafer are subject to significant polymerisation and there is a need for frequent plasma cleans which greatly reduce the throughput.
- It is difficult to control the etched profile by varying the process parameters.

It is possible to increase the volatility of the In by using a Cl_2 based process gas and a high temperature ESC. The etch product becomes $InCl_3$ and both smooth surfaces and steep profiles result. Figure 2 shows a feature etched into InP at a platen temperature of 40 ^oC (wafer temperature ~65 ^oC) using a silicon oxide hard-mask. The etched profile of ~63° is typical of that which results from a sputter dominated process, despite the process chemistry being Cl_2/Ar. At platen temperatures above ~150 ^oC, however, the etch mechanism changes to one of ion assisted chemistry and the etch profile steepens to ~85-90° depending on the precise process conditions. High temperature processes necessitate the use of a hard-mask that is usually silicon oxide. Figure 3 shows a shallow waveguide etched into InP using a $Cl_2/Ar/N_2$ process at a platen temperature of 180 ^oC

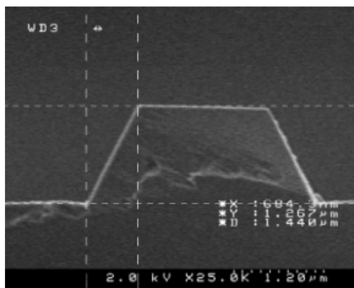

Figure 2 Shallow feature in InP etched at 40 ^oC.
Profile ~63°.

Here the InP etch rate is ~1.6 µm/min and the resulting profile of ~85° is optimum for use as a waveguide. The selectivity of InP to the silicon oxide mask is ~16:1.

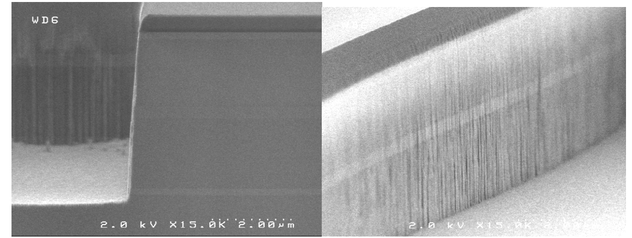

Figure 3 Shallow feature through an epitaxial stack containing InGaAs, InP and InGaAsP etched at 180 ^oC. Profile ~85°.

From the SEM pictures the horizontal and vertical etched surfaces appear to be smooth enough for low loss waveguiding but this will need to be confirmed in the future by optical assessments.

Figure 4 shows an example of a deep etch process which can be used to form an optical mirror. Here the etch depth is ~6 µm (but it is likely to be deeper in the final device) and etching proceeds through a number of epitaxial layers. The Cl_2/N_2 process at 150 ^oC used in this case results in a vertical profile with relatively smooth sidewalls and a smooth 'floor'. It is particularly interesting to notice that the bottom corners of the etch form almost perfect right angles. This is unusual for such processes, where no etch stop layer is used, but is beneficial to the overall performance of the feature as an optical mirror. The InP etch rate and the selectivity to the oxide mask were 1.0 µm/min and ~15:1 for this process.

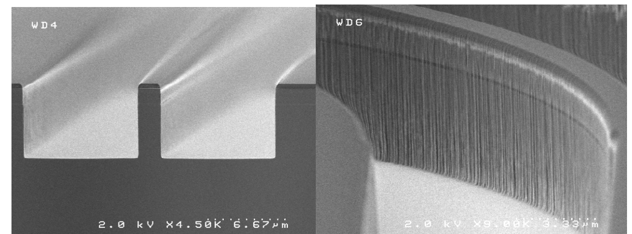

Figure 4 Deep optical mirror feature through an epitaxial stack containing InGaAs, InP and InGaAsP etched at 150 ^oC. Profile ~90°.

Dielectric Etching

As we have already seen, dielectrics may conveniently be used as sacrificial hard-masks for InP etching at elevated temperatures. Dielectrics are also used for subsequent contacting by metals to various parts of the optoelectronic device. For dielectric etching it is convenient to use photoresist masks and fluorocarbon gases as the final etch products (such as SiF_4, CO_2 and COF_2) are sufficiently volatile to be etched at or around room temperature. The following issues are important when etching dielectrics :

- The etch rate needs to be fast enough for a production process.
- The profile needs to be accurately controlled as this will influence its performance as a hard-mask or the subsequent metal coverage.

- The selectivity to the underlying semiconductor needs to be high enough so that there is either negligible loss or a consistent loss (for hard-masks).

The Omega M0RI system is better suited to dielectric etching than the ICP. The helicon wave of the M0RI produces a higher density of ions above the wafer than the ICP. As dielectric etching relies upon significant ion assistance to the fluorocarbon chemistry (due to the strong nature of the Si-O bonding) the M0RI approach is able to achieve higher etch rates and better selectivity and uniformity control.

Hard-mask Open Processes

The wafers used for these experiments had the following layer structure :

~1.2 µm patterned photoresist/6000 Å silicon oxide/InP

Two M0RI etch processes were compared for profile and edge roughness. Both processes were run at 2.5 mtorr and at constant RF power levels. The results are shown in Table I.

TABLE I
RESULTS OF HARD-MASK OPEN M0RI ETCH PROCESSES

Process	Gases	Oxide etch rate (Å/min)	Selectivity to resist	Profile (^{o})
#1	C_4F_8/CH_2F_2	3930	2.7:1	85±1
#2	C_4F_8	5480	1.4:1	82-83

Figures 5 and 6 are the corresponding SEM pictures.

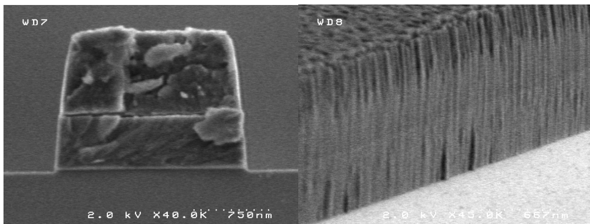

Figure 5 Oxide hard-mask open process using C_4F_8/CH_2F_2.

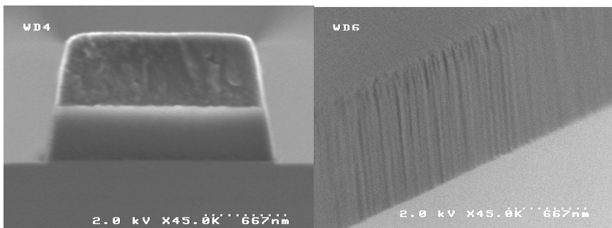

Figure 6 Oxide hard-mask open process using C_4F_8 only.

CH_2F_2 is a heavily polymerising gas and so it is understandable that by removing it from the chemistry the process becomes less anisotropic, less selective to the resist and faster. The improved sidewall roughness of the C_4F_8 only process makes this the best choice for device fabrication despite the slightly shallower profile and poorer resist selectivity. This process also benefits through having a ~40 % higher etch rate. Figures 5 and 6 show that there is some loss of the underlying semiconductor but this is not important as the semiconductor is subsequently etched using the hard-mask.

Sidewall 'Spacer' Etching

A sidewall 'spacer' etch process is an ideal way of forming a contact to the top of a ridge (eg. for use in fabricating ridge waveguide lasers). The wafers used for these experiments had the following layer structure :

~2.5 µm patterned photoresist/2.3 µm silicon oxide/InP topography.

In addition to the previous requirements it is necessary to remove the oxide from the ridge without producing a significant step in the oxide at the ridge top. For some applications it is necessary to simultaneously define the oxide in other device areas for subsequent use as a hard-mask. Figure 7 shows the result of a 2 step M0RI process. The first step uses C_4F_8 only, giving an etch rate of ~6060 Å/min, whereas the second step introduces CH_2F_2 in order to improve the selectivity to the InP underlayer. The oxide etch rate for the second step is ~3250 Å/min.

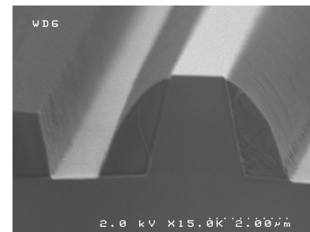

Figure 7 Sidewall 'spacer' etch using 2 step process.

The resulting step at the top of the ridge is <0.1 µm and the oxide profile in planar regions away from topography is ~82° making it an appropriate hard-mask. Both dielectric etch processes were end-pointed by monitoring the optical emission at 440 nm (SiF^*).

CONCLUSIONS

Practical and manufacturable dry etch processes, based on high density plasma systems, have been demonstrated that meet the needs of the optoelectronics industry. ICP processes, using a hot ESC, have been used for both shallow waveguide and deep mirror etches. M0RI processes, using a conventional low temperature ESC, have been used for dielectric hard-mask open and 'spacer' etching. Future work will concentrate on the benefits that these processes bring to the final optoelectronic device performance.

REFERENCES

1. Y P Song, A Watson, D J Thomas, K Powell, H-E Raske, W-D Domke & M Sebald, Electrochemical Society Proceedings, **99-30**, 226 (2000).
2. D A Tossell, K Powell, M M Bourke and Y P Song, GaAs Mantech, Washington 2000.